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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,246	11/15/2000	Tetsushi Tanizaki	49657-875	8725

20277 7590 01/27/2005

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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/712,246	TANIZAKI ET AL.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments/amendments with respect to previously presented claims 1-16 filed October 19, 2004 have been fully considered but are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, "...Adams et al. (prior art of record) does not teach the ALPG configured for generating test data based on the address signal." The Examiner respectfully disagrees. Adams patent deals with a memory Array Built-In Self-Test (ABIST) circuit that tests a multi-port memory array. A programmable pattern generator for the ABIST circuit allows for different R/W data operations to be performed at the same or adjacent address locations within a multi-port memory array. Adams teaches the programmable pattern generator comprises a data generator, a read/write controller, and an address counter, each having the same number of outputs as ports of the multi-port memory array. The programmable pattern generator also comprises a frequency controller. The data generator is programmed with the appropriate data patterns for the memory array, and the read/write controller is programmed with the appropriate read/write patterns for the memory array. The address counter is to provide the same or different addresses on each port of the multi-port array, and the frequency controller is programmed with the appropriate frequency information to determine the number of read/write operations per cell in the memory array. The combination of programmable data, programmable read/write sequences, programmable address counter, and programmable frequency allows for determistic testing of a multi-port memory array, a plurality

of single-port memory arrays, or a combination thereof by providing unique read/write sequences to the same or to adjacent memory locations. Adams teaches a programmable pattern generator in the ABIST circuit allows for different Read/Write (R/W) data operations to be performed at the same or adjacent address locations within a multi-port memory array. The programmable pattern generator comprises a data generator, a read/write controller, and an address counter, each having the same number of outputs as ports of the multi-port memory array. The programmable pattern generator also comprises a frequency controller, which provides the clock signal to the address counter. Particularly, the data generator is programmed with the appropriate data patterns for the memory array, and the read/write controller is programmed with the appropriate read/write patterns for the memory array. The address counter is programmed to invert or not invert specific port address bits, and the frequency controller is programmed with the appropriate frequency information to determine the number of read/write operations performed at each memory address. The combination of programmable data, programmable read/write sequences, and the ability to program whether each port receives the same address or different addresses allows for deterministic testing of a multi-port memory array, or even several single port memory arrays, by providing unique read/write sequences to the same and to adjacent cells.

The Examiner disagrees with the Applicant and maintains rejections with respect to previously presented claims 1-16. All arguments have been considered. It is the Examiner's conclusion that previously presented claims 1-16 are not patentably distinct or non-obvious over the prior art of record. See prior office action herein above.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lepejian et al (USPN 5974579) further in view of Adams et al. (USPN 5796745). See prior action below.

As per claim 1, Lepejian et al (herein after: Lepejian) substantially teaches (title & abstract) a method and apparatus for testing a semiconductor memory using a built-in self-test (BIST) circuit. Lepejian teaches to test circuits built into the semiconductor integrated circuit that enable efficient testing of embedded memory, especially read/write memory. Lepejian teaches a built-in self-test circuit for testing one or more embedded memories by writing data to each memory address (analogous to memory cell in the present application), reading it back, and then comparing the input and output data to see if they match. **The BIST circuit includes a data generator (analogous to test circuit in the present application) for supplying a sequence of data (analogous to test data) to be written to the various addresses of the memory during read and write operations**. Lepejian teaches (col. 2, lines 15-19) the option of having an input buffer that receives externally applied data. Lepejian teaches (col. 3, lines 62-68—col. 4, lines 1-3) a routing technique to strategically apply test data to the memory. The routing area devoted to address lines used in accessing the embedded memories is minimized by generating the address

locally at each memory with a pseudo-random generator based on a clocked shift register with linear feedback defined by a primitive polynomial. The address routing requires only control signals to the local generators, and the generators themselves are very efficient in terms of layout area and capable of operating at the maximum circuit frequency. The Examiner would like to point out that the functionality of the select circuit of the present application is included in the teachings of Lepejian, as detailed above. Furthermore, Lepejian teaches (col. 2, line 34) the memory to operational in both test and normal modes as stated in the present application. Lepejian teaches (col. 2, lines 45-55) an implementation which involves adding a series of control lines so that each memory can be enabled separately. This allows each memory to be tested sequentially. Lepejian teaches (figure 1) a main controller, which is responsible for coordinating and synchronizing the tests that are conducted on the memory array. Referring to figure 1 of Lepejian, decoder 85 decodes the encoded data on bus 11 from main controller 10 and provides decoded data to local de-skewing circuit 70, which passes the data on decoded data bus 81 to the memory under test. Address generator 40 receives address clock 13, address initialization signal 14, address reset signal 15, and increment or decrement signal 16 from main controller to generate the addresses used in accessing memories. The generated addresses are also provided to de-skewing circuit 70. Local timing de-skewing circuit provides pulse shaping and edge placement for the input signals to each embedded memory array. The signals on address bus 84, control line 83 and decoded data bus 81 test the memories under test by writing and reading from all of the memory locations in both polarities with differing address sequences. De-skewing circuit assures that there are no timing problems associated with accessing different embedded memory arrays that may be separated by more than a centimeter on the integrated

circuit chip. Furthermore, the de-skewing circuit in figure 4 employs synchronously clocked latches to provide the de-skewing function. Lepejian teaches (col. 2, lines 30-45) to add multiplexers to the memory input/output lines such that the data read from the memory can be loaded back into adjacent bits during the subsequent write while the memory is in the test mode. In operational mode, the multiplexers connect the memory data lines to the chip data bus. Because data is always available for writing when a read operation is completed, the memory may be tested at various operational speeds, which increases the quality and accuracy of the test procedure.

Lepejian does not explicitly teach the BIST circuit to comprise of a programmable algorithmic pattern generator as stated in the present application.

However, Adams et al. (herein after: Adams) substantially teaches (title and abstract) a memory Array Built-In Self-Test (ABIST) circuit that tests a multi-port memory array. **In particular, Adams teaches a programmable pattern generator for the ABIST circuit allows for different R/W data operations to be performed at the same or adjacent address locations within a multi-port memory array. The programmable pattern generator comprises a data generator, a read/write controller, and an address counter, each having the same number of outputs as ports of the multi-port memory array.** The programmable pattern generator also comprises a frequency controller. The data generator is programmed with the appropriate data patterns for the memory array, and the read/write controller is programmed with the appropriate read/write patterns for the memory array. The address counter is to provide the same or different addresses on each port of the multi-port array, and the frequency controller is programmed with the appropriate frequency information to determine the number of read/write

operations per cell in the memory array. The combination of programmable data, programmable read/write sequences, programmable address counter, and programmable frequency allows for determinstic testing of a multi-port memory array, a plurality of single-port memory arrays, or a combination thereof by providing unique read/write sequences to the same or to adjacent memory locations. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a programmable pattern generator within the BIST circuit of Lepejian. This modification in testing the memory would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by including a programmable patterns generator within the BIST circuit of Lepejian would allow for more rigorous testing of port arbitration and memory address sensitivities (including cell-to-cell, bitline-to-bitline, and wordline-to-wordline coupling sensitivities).

As per claims 2-10, Lepejian substantially teaches, in view of above rejections (col. 1, lines 14-15) an instruction cache memory on the semiconductor substrate. A test pattern generation circuit (figure 1) is also included in the main controller to generate test patterns and apply them to the memory under test according to specific instructions. Lepejian teaches (figure 1) the circuitry for a BIST function that can typically be generated by a logic synthesizer that receives input files in a high-level design language (analogous to program instructions in the present application) describing the function to be performed. Main controller 10 (analogous to controller) controls the testing operation. The blocks that are distributed for the BIST function are address generator 40, address filter 50, data decoder 85, data comparator 80 and local timing de-skewing circuit 70, each directly coupled to main controller 10. In the present application, the applicant states that the operation of the test pattern generation circuit, instruction memory,

memory cell array and the read-out circuit is synchronized with a frequency-multiplied by a predetermined factor. The examiner would like to point out—in view of above rejections—that the testing of a memory under various operational frequencies would actually enable test pattern generation circuit, instruction memory, memory cell array and the read-out circuit to be in synchronous with a factor of the original frequency. In other words, testing a memory under different frequencies would automatically mean that the change in the frequency—increase or decrease—would change the rate of testing components as well.

As per claims 11-16, Lepejian substantially teaches, in view of above rejections, (col. 2, lines 30-45) to add multiplexers to the memory input/output lines such that the data read from the memory can be loaded back into adjacent bits during the subsequent write while the memory is in the test mode. In operational mode, the multiplexers connect the memory data lines to the chip data bus. Because data is always available for writing when a read operation is completed, the memory may be tested at various operational speeds, which increases the quality and accuracy of the test procedure. Lepejian teaches (col. 1, lines 14-15) an instruction cache memory (analogous to rewritable instruction memory in the present application) on the semiconductor substrate. A test pattern generation circuit (analogous to algorithm pattern generator) is also included in the main controller to generate test patterns and apply them to the memory under test according to specific instructions (figure 1 Lepejian). Furthermore, Lepejian teaches (col. 2, lines 15-19) the option of having an input buffer that receives externally applied data, as stated before. The examiner would like to point out that the testing of the memory device in the first and second level in the present application is analogous to testing under first and second frequencies.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
January 12, 2005

Guy J. Lamarre
Primary Examiner